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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,791	06/30/2003	Xiaoning Ye	42P15581	1296
8791	7590	04/13/2005	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			NATALINI, JEFF WILLIAM	
			ART UNIT	PAPER NUMBER
			2858	

DATE MAILED: 04/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/611,791		YE ET AL.	
	<b>Examiner</b>		<b>Art Unit</b>	
	Jeff Natalini		2858	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 February 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-6,8-13,15-21,23 and 24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6,8-13,15-21,23 and 24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>2/28/05</u> . | 6) <input type="checkbox"/> Other: _____  |

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-6, 8-11, 13, 15, 17, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhu et al. (6856210- which is the patent given to application US 2001/054939).

In regard to claims 1, 8, 13, and 23, Zhu et al. teaches a circuit board/method of forming (abstract) comprising: at least one signal trace disposed on a dielectric layer (fig 1 shows dielectric substrates with traces; col 3 line 26-31), wherein the signal trace comprises a first width that is wider than the second width (fig 7 (first width 405 – second width (404))); at least one via electrically connected to the first width of the at least one signal trace (fig 7 (410)) electrically connecting a circuit component (via hole/transmission line) to the via (col 3 line 14-22; and it is known in the art that components are connected to the board/vias in order to transfer signals from one component to another);

Zhu et al. lacks specifically stating that the impedance discontinuity between the trace and a component is lowered from above about 5 ohm to less than about 1 ohm.

Zhu et al. provides an adjustable impedance matching planar circuit between the via hole and the signal transmission line (col 3 line 19-22) that is adjusted by

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changing widths and lengths of the signal line (abstract) for use in high frequency multilayer circuit substrates used in a microwave band (col 1 line 6-9) for reducing impedance of electrical connection (abstract).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Zhu et al. to lower the impedance discontinuity between the signal trace and a component from about 5 ohms to less than 1 ohm to lower the impedance of the electrical connection in order to use the circuit substrate in a high frequency microwave band (col 1 line 6-9) as it is known in the art to ideally have the impedance of the electrical connection as close to zero as possible to avoid transmission loss.

In regard to claims 2, 9, and 24, Zhu et al. discloses wherein the ratio of the first width to the second width is about 2:1 to 3:1 (col 5 line 5-15, width 1 =  $180\mu$  and width 2 =  $100\mu$ m so the ratio is 1.8:1 which is about 2:1).

In regard to claim 3, Zhu et al. discloses wherein the first width is located in a anti-pad region, wherein the signal trace extends from the center of the via to slightly past the edge of the anti-pad region (fig 1, via (110), is in the antipad region, which surrounds the via, and approximately ends at the end of the first width seen by the box to the left of 13).

In regard to claim 4, Zhu et al. discloses wherein the second width is located in a ground plane region wherein the ground plane region extends slightly past the edge of the anti-pad region to the end of the signal trace opposite the first width (fig 1, ground

plane region is seen to the left and right of the via, as seen by the traces formed in this area-avoiding the area around the via (anti-pad)).

In regard to claim 5, Zhu et al. discloses wherein the signal trace further comprises a via pad (fig 7 (402)),

In regard to claim 6, Zhu et al. discloses wherein the first width is not substantially disposed over a ground plane (seen in fig 1; first width (box to the left of where 13 is pointing) is mostly in anti-pad region).

In regard to claim 10, Zhu et al. discloses wherein the first width is located in a signal trace anti-pad region (fig 1, can see first width connected to via (left of where 13 is pointing), second width is to the right of first width and is in the ground region- also see rejection of claims 4 and 5 above).

In regard to claim 11, wherein the at least one signal trace is not substantially disposed over an underlying ground plane in a anti-pad region (fig 1, can see first width connected to via (left of where 13 is pointing), second width is to the right of first width and is in the ground region- also see rejection of claims 4 and 5 above).

In regard to claim 15, wherein the component is adapted for receiving a signal (abstract; signals will run through the path into the component).

In regard to claim 17, wherein the signal has a frequency of above about 5 GHz (fig 6 and fig10).

3. Claims 16, 18, 19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhu et al. (6856210), as applied to claim 15 above (for claim 16), and in view of Arabi (6501278).

In regard to claims 16, 18, and 21, Zhu et al. teaches a circuit board/method of forming (abstract) comprising: a ground pad disposed on a dielectric layer (fig 1 (211)-ground pad fig 3 (201); col 3 line 49-56); at least one signal trace disposed on the dielectric layer (fig 1 shows dielectric substrates with traces; col 3 line 26-31), wherein the signal trace comprises a first width that is wider than the second width (fig 7 (first width 405 – second width (404))); at least one via electrically connected to the first width of the at least one signal trace (fig 7 (410)) electrically connecting a circuit component (via hole/transmission line) to the via (col 3 line 14-22; and it is known in the art that components are connected to the board/vias in order to transfer signals from one component to another);

Zhu et al. lacks a TDR prober including a signal output and a signal ground, and wherein the ground pad is specifically coupled to the signal ground.

Arabi teaches a TDR probing system that includes a signal output and a signal ground (abstract second sentence) for use in circuit board testing (abstract); and teaches the use of a ground pad formed on the first surface of the substrate under test and the ground pad is connected to the ground plane (abstract).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Zhu et al. to have a TDR probing system with a signal output and signal ground, and where the ground pad is grounded as taught by Arabi in order to have minimal impedance discontinuities at high frequencies (col 3 line 25-27).

In regard to claim 19, Zhu et al. discloses wherein the ratio of the first width to the second width is about 2:1 to 3:1 (col 5 line 5-15, width 1 = 180 $\mu$  and width 2 = 100 $\mu$ m so the ratio is 1.8:1 which is about 2:1)

4. Claims 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhu et al. (6856210) and Arabi (6501278), further in view of Arabi (6501278) as applied to claims 8 and 18 above, and further in view of Pon (4517535).

In regard to claims 12 and 20, Arabi as modified lacks wherein the component is one of a SMA, BNC, or SIP connector.

Pon teaches using a SMA connector for transferring signals from a signal line device to a circuit board trace (col 10 line 57-61).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Govind et al. and Klaassen to use a SMA as the component as taught by Pon in order to connect high frequency signals from a signal line device to a circuit board trace (col 10 line 60-61).

### ***Conclusion***

5. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on February 28, 2005 prompted the new ground(s) of rejection presented in this Office action (The PTO-892 attached is the three patents that were granted from the publications 2001/0054939, 2001/0051210, and 2002/0040809 (from the IDS filed 2/28/05) so that they may appear on the record).

Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Natalini whose telephone number is 571-272-2266. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lefkowitz can be reached on 571-272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeff Natalini



**ANJAN DEB**  
**PRIMARY EXAMINER**